In the Claims

Claims 1-24 are canceled.

Cancel claims 31-37.

25.   [Original] A computer system comprising:

a central processing unit;

an input interface coupled to the central processing unit; and a memory device coupled to the central processing unit, the memory device storing instructions and data for use by the central processing unit, wherein the memory device includes a SRAM array formed from cells each including in combination:

a first load device;

a first ultrathin transistor having a power electrode coupled to the first load device;

a second load device; and

a second ultrathin transistor including a power electrode coupled to the second load device, wherein the first load device is merged with a control electrode of the second ultrathin transistor and vice versa.

26.   [Original] The computer system of claim 25, wherein the first ultrathin transistor comprises a vertical NMOS FET and the second ultrathin transistor comprises a vertical PMOS FET.

27.   [Original] The computer system of claim 25, wherein the first transistor has a load electrode coupled to a row address line and the first load device is coupled to a column address line.

28.   [Original] The computer system of claim 25, wherein the first and second transistors comprise polycrystalline semiconductor material.

29.   [Original] The computer system of claim 25, wherein the first and second transistors comprise FETs each having a gate electrode, and the first load device is merged with the gate of the second transistor and the second load device is merged with the gate of the first transistor.

30.   [Original] The computer system of claim 25, wherein each cell comprises an area of 8F2, or less, wherein F represents one-half of a minimum lithographic pitch of the SRAM cell.

38.   [Original] A process for turning a SRAM cell OFF comprising increasing a voltage applied to a switch in the SRAM cell above a threshold voltage for that switch.

39.   [Original] The process of claim 38, wherein the act of turning a SRAM cell OFF comprises turning a row of SRAM cells OFF.

40.   [Original] The process of claim 38, wherein the SRAM cell comprises a first transistor and a second transistor, wherein the switch comprises the second transistor and wherein the second transistor comprises an ultrathin NMOS transistor having a gate, a source, a drain and a threshold voltage, the source being coupled to a row address line and the drain being coupled to a column address line and wherein the act of turning a SRAM cell OFF comprises raising a voltage coupled to the row address line above the threshold and turning a row of SRAM cells coupled to that row address line OFF.

41.   [Original] The process of claim 38, wherein the act of turning a SRAM cell OFF comprises turning OFF all of the transistors in that cell.

42.   [Original] The process of claim 38, wherein the first transistor comprises an ultrathin PMOS transistor having a gate, a source and a drain and the switch comprises the second transistor, the second transistor comprising an ultrathin NMOS transistor having a gate, a source and a drain, the NMOS transistor source being coupled to a row address line and the NMOS transistor drain being coupled to a column address line and wherein the act of turning a SRAM cell OFF comprises:

raising a voltage coupled to the row address line above the threshold and turning the NMOS transistor coupled to that row address line OFF; and

causing a source-drain voltage of the PMOS transistor to become less than a threshold voltage for the PMOS transistor in response to the NMOS transistor turning OFF.

43.   [Original] The process of claim 38, wherein the SRAM cell is coupled to a row address line and wherein the act of turning a SRAM cell OFF comprises raising a voltage coupled to the row address line from about zero volts to about 0.7 volts or less.

44.   [Original] The process of claim 38, wherein the act of turning a SRAM cell OFF comprises turning OFF both of the two transistors in that cell.

45.   [Original] A process for writing a SRAM cell comprising two switches, where one of the two switches is coupled to a row address line and a column address line, to an ON state, comprising modifying a voltage coupled to the row address line to cause a voltage applied to a control electrode of the one switch to exceed a threshold voltage for that switch.

46.   [Original] The process of claim 45, further comprising modifying voltages coupled to column address lines of SRAM cells that are not to be written to the ON state to prevent the row address line voltage modification from turning ON switches in the SRAM cells that are not to be written to the ON state.

47.   [Original] The process of claim 46, wherein modifying voltages coupled to column address lines comprises raising the voltages coupled to the address lines of SRAM cells that are not to be written to the ON state.

48.   [Original] The process of claim 45, wherein at least one of the two switches comprises a NMOS FET having a gate, drain, source and threshold voltage VTN, wherein the source is coupled to the row address line and the drain is coupled to the column address line, wherein modifying a voltage coupled to the row address line comprises reducing the voltage coupled to the row address line below ground to cause a voltage applied to the gate to exceed the threshold voltage VTN.

49.   [Original] The process of claim 45, further comprising, prior to modifying a voltage, writing a row of SRAM cells coupled to the row address line to the OFF state.

50.   [Original] A process for reading data from a SRAM cell including a first transistor of a first conductivity type and a second transistor of a second conductivity type comprising:

increasing a voltage across a portion of the cell including two power electrodes of one of the first and second transistors; and

monitoring a current through the power electrodes of the one transistor.

51.   [Original] The process of claim 50, wherein increasing comprises increasing the voltage by less than an amount represented by a turn-on voltage of the one transistor.

52.   [Original] The process of claim 50, wherein the first transistor comprises an ultrathin PMOS transistor and the second transistor comprises an ultrathin NMOS transistor, and wherein:

increasing comprises lowering a voltage impressed on a source of the NMOS

transistor below a ground reference voltage; and

monitoring comprises monitoring a drain current of the NMOS transistor.

53.   [Original] The process of claim 50, further comprising:

determining that a first logical state was stored in the SRAM cell when no current

increase accompanies increasing; and

determining that a second logical state different than the first logical state was

stored in the SRAM cell when a current increase accompanies increasing.

54.   [Original] The process of claim 50, wherein the first transistor comprises an

ultrathin PMOS transistor having a gate, a source and a drain and the second transistor

comprises an ultrathin NMOS transistor having a gate, a source and a drain, the NMOS

transistor source being coupled to a row address line and the NMOS transistor drain being

coupled to a column address line and wherein:

increasing comprises reducing a potential applied to the row address line; and

monitoring comprises monitoring a current through the column address line.

55.   [Original] The process of claim 50, wherein the first transistor comprises an

ultrathin PMOS transistor having a gate, a source and a drain and the second transistor

comprises an ultrathin NMOS transistor having a gate, a source and a drain and wherein

increasing comprises increasing a gate-source voltage of the NMOS transistor to a value

that is less than a threshold voltage of the NMOS transistor.